**ARM Embedded Systems**

ARM History:

* First ARM was developed by **Acorn Computers Limited**, Cambridge between 1983 & 1985
  + **First commercial RISC Processor**
* In 1990, the company named **Advanced RISC Machines Limited** was formed
* Later it was renamed as **ARM Limited**
* ARM has been licensed to many semiconductor manufacturers like:
  + **National Semiconductor**
  + **Philips**
  + **Atmel,etc**

**ARM Powered Products**:





**RISC Design Philosophy**:

* Is based on simple instructions that execute within a single cycle at a high clock speed.
* 4 major design rules

1. Instructions
2. Registers
3. Pipelining
4. Load and store architecture.

1) Instructions :

* Mostly single cycled instructions, except for few.
* The Compiler or programmer synthesizes complicated instructions.
* Having fixed length which helps in pipelining.

2) Pipelining:

* The processing of instructions is broken down into smaller units that can be executed in parallel by pipelines.
* Maximizes throughput.

3) Registers :

* Large general-purpose register set.
* Any register can contain either data or an address.
* Registers act as the fast local memory store for all data processing operations.

4) Load-store architecture :

* Register Intensive processing
* The processors operate on data held in registers. Separate load and store instructions transfer data between the register bank and eternal memory.Memory accessing are costly,so separating memory accesses from data processing provides an advantage because you can use data items held in the register bank multiple times without needing multiple memory accesses.

ARM architectural features:

* An ARM processor is one of a family of [CPUs](https://whatis.techtarget.com/definition/processor) based on the [RISC](https://whatis.techtarget.com/definition/RISC) (reduced instruction set computer) architecture developed by Advanced RISC Machines (ARM).
* ARM makes 32-bit and [64-bit](https://searchdatacenter.techtarget.com/definition/64-bit-processor) RISC [multi-core processors](https://searchdatacenter.techtarget.com/definition/multi-core-processor).
* RISC processors are designed to perform a smaller number of types of computer [instructions](https://whatis.techtarget.com/definition/instruction) so that they can operate at a higher speed, performing more millions of instructions per second ([MIPS](https://searchitoperations.techtarget.com/definition/MIPS-million-instructions-per-second)).  By stripping out unneeded instructions and optimizing pathways, RISC processors provide outstanding performance at a fraction of the power demand of [CISC](https://whatis.techtarget.com/definition/CISC-complex-instruction-set-computer-or-computing) (complex instruction set computing) devices.
* ARM processors are extensively used in consumer electronic devices such as [smartphones](https://searchmobilecomputing.techtarget.com/definition/smartphone), [tablets](https://searchmobilecomputing.techtarget.com/definition/tablet-PC), multimedia players and other mobile devices, such as [wearables](https://internetofthingsagenda.techtarget.com/definition/wearable-computer). Because of their reduced [instruction set](https://whatis.techtarget.com/definition/instruction-set), they require fewer [transistors](https://whatis.techtarget.com/definition/transistor), which enables a smaller die size for the integrated circuitry (IC).
* The ARM processor’s smaller size, reduced complexity and lower power consumption makes them suitable for increasingly miniaturized devices.
* ARM has hardware debug technology within the processor so that software engineers can view what is happening while the processor is executing code. With greater visibility ,software engineers can resolve issues faster,which has direct effect on the time to market and reduces overall development cost.
* 37 registers
  + 31 general 32 bit registers, including PC
  + 6 status registers
  + 15 general registers (R0 to R14), and one status registers and program counter are visible at any time
* –when you write user-level programs

•R13 (SP)

•R14 (LR)

•R15 (PC)

* The visible registers depend on the processor mode.

ARM core 7 modes of operation:

* **User (usr):** Normal program execution state.
* **FIQ (fiq):** Data transfer state (fast irq).
* **IRQ (irq):** Used for general interrupt handling.
* **Supervisor (svc):** Protected mode for operating system support.
* **Abort mode (abt):** Selected when data or instruction fetch is aborted.
* **System (sys):** Operating system ‘privilege’-mode for user.
* **Undefined (und):** Selected when undefined instruction is fetched.